CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller, comprising:

a built-in self-test engine capable of executing a built-in self-test and generating an indication of whether the executed built-in self-test is completed; and

a built-in self-test signature including the indication.

2. The built-in self-test controller of claim 1, wherein the built-in self-test engine is a logic built-in self-test engine and the built-in self-test signature is a logic built-in self-test signature.

3. The built-in self-test controller of claim 2, wherein the logic built-in self-test engine comprises:

a logic built-in self-test state machine; and

a pattern generator.

4. The built-in self-test controller of claim 3, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

5. The built-in self-test controller of claim 1, wherein the logic built-in self-test signature comprises the content of a multiple input signature register.

6. The built-in self-test controller of claim 1, wherein the built-in self-test engine is a memory built-in self-test engine and the built-in self-test signature is a memory built-in self-test signature.

7. The built-in self-test controller of claim 6, wherein the memory built-in self-test signature includes the results of at least one paranoid check..

8. The built-in self-test controller of claim 6, wherein the memory built-in self-test signature includes a bit indicating whether a memory built-in self-test is done.

9. The built-in self-test controller of claim 6, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

10. The built-in self-test controller of claim 9, wherein the memory built-in self-test state machine comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

11. The built-in self-test controller of claim 9, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

12. The built-in self-test controller of claim 11, wherein each of the memory built-in self-test engines comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

13. A built-in self-test controller, comprising:

means for executing a built-in self-test and generating an indication of whether the executed built-in self-test is completed; and

means for storing the results of the executed built-in self-test, including the indication.

14. The built-in self-test controller of claim 13, wherein the executing means is a logic built-in self-test engine and the storing means is a logic built-in self-test register.

15. The built-in self-test controller of claim 13, wherein the storing means comprises the content of a multiple input signature register.

16. The built-in self-test controller of claim 13, wherein the executing means is a memory built-in self-test engine and the storing means is a memory built-in self-test signature register.

17. An integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

a built-in self-test engine capable of executing a built-in self-test on one of the memory components and the logic core and storing the results thereof, wherein the results include an indication of whether an executed built-in self-test is completed; and

a register capable of storing the results of an executed built-in self-test, including the indication.

18. The integrated circuit device of claim 17, wherein the built-in self-test engine is a logic built-in self-test engine and the register is a multiple input signature register.

19. The integrated circuit device of claim 17, wherein the built-in self-test engine is a memory built-in self-test engine and the register is a memory built-in self-test signature register.

20. The integrated circuit device of claim 17, wherein the memory components include a static random access memory device.

21. The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.

22. A method for performing a built-in self-test, the method comprising:

performing a built-in self-test, including generating a indication of whether the built-in self-test is completed; and

storing the indication.

23. The method of claim 22, wherein performing the built-in self-test includes performing a logic built-in self-test and storing the indication includes setting a bit in a multiple input signature register.

24. The method of claim 23, wherein performing the logic built-in self-test includes:

resetting a logic built-in self-test engine;

initiating a plurality of components and signals in a built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator in a logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count.

25. The method of claim 23, further comprising at least one of:

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

26. The method of claim 22, wherein performing the built-in self-test includes performing a memory built-in self-test and storing the indication includes setting a bit in a memory built-in self-test signature register.

27. The method of claim 26, wherein performing the memory built-in self-test includes:

resetting a memory built-in self-test engine;

initiating a plurality of components and signals in a built-in self-test controller upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals; and

testing the flushed memory components.

28. The method of claim 26, wherein performing the memory built-in self-test further includes at least one of:

storing the results of the memory built-in self-test in the memory built-in self-test signature register; and

storing the results of at least one paranoid check in the memory built-in self-test signature register.

29. A method for testing an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a built-in self-test, including generating a indication of whether the built-in self-test is completed;

storing the indication; and

reading the indication.

30. The method of claim 29, wherein performing the built-in self-test includes performing a logic built-in self-test and storing the indication includes setting a bit in a multiple input signature register.

31. The method of claim 29, wherein performing the built-in self-test includes performing a memory built-in self-test and storing the indication includes setting a bit in a memory built-in self-test signature register.

32. The method of claim 29, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.